IN THE CLAIMS:

Please cancel claims 5-6 without prejudice, amend claim 1 as follows:

- 1. (Currently Amended) A peripheral or memory device having a bus, and a bus switching circuit that comprises:
 - a first bus decoder circuit coupled to the bus for decoding signals in a first format;
- a second bus decoder circuit coupled to the bus for decoding signals in a second format:
 - a first bus snoop circuit coupled to the bus;
 - a second bus snoop circuit coupled to the bus;
- a switch coupled to the first bus snoop circuit for receiving a first bus detect signal therefrom, and the switch coupled to the second bus snoop circuit for receiving a second bus detect signal therefrom; [[and]]

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of the first and second detect signals; and

wherein the switch, the first bus snoop circuit and the second bus snoop circuit are separated from each other.

- 2. (Original) The device of claim 1, wherein the first bus decoder circuit is an ISA bus decoder circuit, and the second bus decoder circuit is an LPC bus decoder circuit.
 - 3. (Previously Amended) A peripheral or memory device comprising:
 - a bus;
- a micro-controller which generates a bus select signal selected by the micro-controller without receiving bus data from the bus; and
 - a bus switching circuit that comprises:
 - a first bus decoder circuit coupled to the bus for decoding signals in a first format;
 - a second bus decoder circuit coupled to the bus for decoding signals in a second format;
 - a switch coupled to the micro-controller for receiving a bus select signal therefrom; and
 - wherein the switch is coupled to the first bus decoder circuit for providing a first bus

enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of the bus select signal.

- 4. (Original) The device of claim 3, wherein the first bus decoder circuit is an ISA bus decoder circuit, and the second bus decoder circuit is an LPC bus decoder circuit.
 - 5-16. (Canceled).
- 17. (Original) The device of claim 1, wherein the first and second bus snoop circuits generate the first and second bus detect signals, respectively, based on a series of I/O writes.